Modeling, Synthesis, and Rapid Prototyping with the VERILOG (TM) HDL

Michael D. Ciletti
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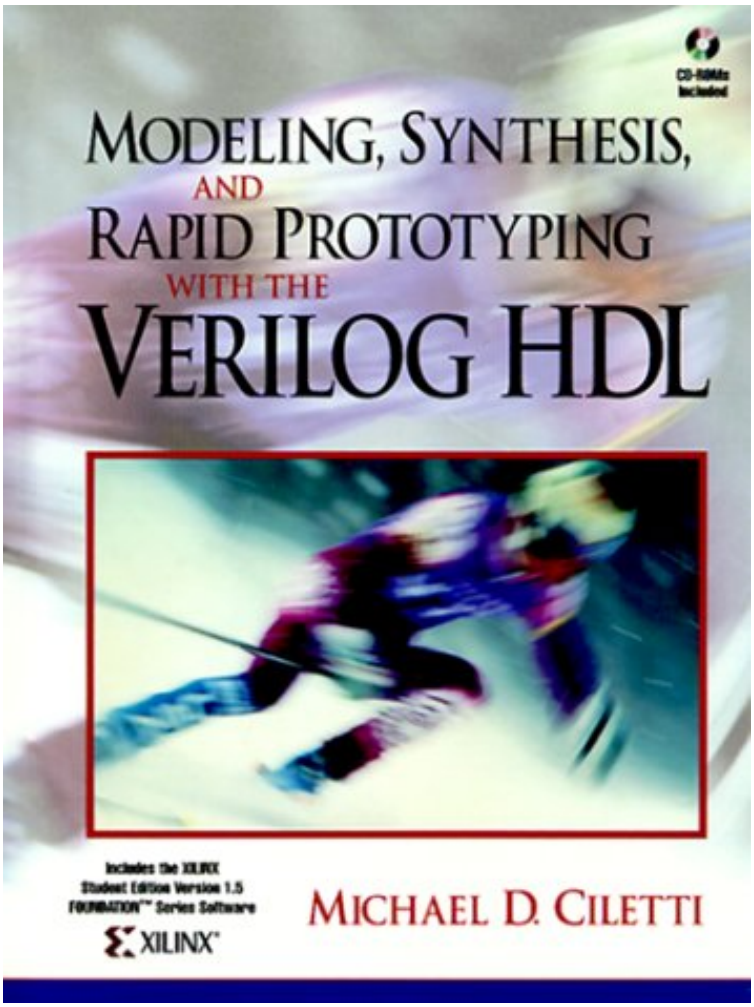

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Michael D. Ciletti : Modeling, Synthesis, and Rapid Prototyping with the VERILOG (TM) HDL before purchasing it in order to gage whether or not it would be worth my time, and all praised Modeling, Synthesis, and Rapid Prototyping with the VERILOG (TM) HDL:

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date. That is not the author's fault, as it was published before Verilog 2001. Everything else *is* his fault, however.This book does not present material in an order that is useful for learning the language. It is not skimmable. It is not easy to just "look something up." Useful information, if there is any, is buried deeply in meaningless exposition. The emphasis placed on the material does not correspond with any design methodology I am familiar with.This book says a log about nothing. Read Sections 8.1 - 8.5, for instance, including such material as "Benefits of Synthesis". Design is about synthesis. Synthesis is the whole *point*.This book uses blocking assignments in sequential logic. It uses nonblocking assignments in combinational logic. This is not just bad style. It is dangerous advice (especially in the former case)Examples in this book are so simple as to be trivial. Examples should be edifying, not obvious.Having been through this book far too many times, now, I am *still* left with no clear idea who it was written for. It is clearly not a practical book for someone looking to pick up Verilog quickly. It certainly has *nothing* to do with rapid prototyping, despite the title. It does not clarify anything that couldn't be more easily gleaned from the Verilog Standard itself.In short, I'm sorry I ever bought this book. It has wasted more of my time than it has ever saved. Instructors: AVOID using this book in your courses, please. Designers, pick somthing else.1 of 1 people found the following review helpful. Recommended.By Stephen HenryI am using this book for an introductory Verilog class at my University and I must say I am truely confused by some of the reviews here. Although this book takes the reader through the most basic elements of the Verilog language, to its more complex and esoteric uses, most people here complain that the it fails to provide the advanced, cutting-edge examples they feel it should have. What? Do you really expect to learn how to build a Pentium IV from a book teaching the basics of Verilog? Get real!This book teaches the basics, it teaches you how to use the Verilog language by providing examples that, although dated, illustrate timeless approaches that are used in every Verilog design large or small. If you can't find how to complement a variable, then its your fault, not the book; I can assure you its there. Furthermore, if you think that pointing out a few mistakes in the book, (and have obviously learnt the correct way of doing it from it), makes it rubbish, then I'm afraid there won't be any books that will fully satisfy your needs.This is one of the best books I've encountered on the Verilog langauge. Although I wouldn't say it's as good as, say, Ashendens VHDL, it is _not_ as bad as some of the reviews here make out. Recommended!

Verilog aims to introduce new users to the language of Verilog with instruction on how to write hardware descriptions in Verilog in a style that can be synthesized by readily available synthesis tools. Offers clear exposition of the Verilog hardware description language. This book is written in a style that allows the user who has no previous background with hardware description languages (HDLs) to become skillful with the language. Features treatment of synthesis-friendly descriptive styles. An excellent book for self-study, reference, seminars, and workshops on the subject.

From the Back Cover Designed for advanced undergraduate and graduate computer science, computer engineering and electrical engineering courses in digital design and hardware description languages, this textbook presents an integrated treatment of the Verilog hardware description language (HDL) and its use in VLSI, circuit modeling/design, synthesis, and rapid prototyping. This product is a selection from the Xilinx Design Series. Back Cover Designers facing the challenge of the next millennium must have the tools to exploit the rapidly advancing technology of cell-based and other ASIC device technologies, such as Field-Programmable Gate Arrays (FPGAs). It is clear that the leverage offered to designers by hardware description languages will continue to shape design methodologies at all levels of integration, from Programmable Logic Devices (PLDs) to Application-Specific Integrated Circuits (ASICs) and full-custom parts. This impact will continue to develop as more designers embrace HDL-based tools. Many of today's design flows for ASICs and FPGAs typically rely on synthesis tools that optimize and map Verilog HDL descriptions into physical netlists, thereby reducing the design cycle while increasing the opportunity for design exploration. The growing acceptance of this design paradigm suggests that an increasing number of designers will need to know how to be productive users of Verilog in the future. This book presents an integrated treatment of the Verilog hardware description language (HDL) and its use in Very Large Scale Integrated (VLSI) circuit modeling/design, synthesis, and rapid prototyping. Included with the text are the SILOS III Verilog development and simulation environment of Simucad, Inc., and the Xilinx Foundation Express Student Edition, Version 2.1, software tools. This suite of PC-based software tools combined with the text makes an invaluable learning environment for digital designers.